Advances in Reversed Nested Miller Compensation

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In this paper, we shall discuss two simple and high-performance compensation strategies, namely the RNMC feedforward with nulling resistor (RNMCFNR) and reversed active feedback frequency compensation (RAFFC).

they are implemented without entailing extra transistors, thus saving circuit complexity and power consumption.

The operational transconductance amplifier (OTA) is a basic building block in most analog and mixed-signal electronic systems.

An increasing number of applications require high-gain high-bandwidth amplifiers able to drive capacitive loads under low-voltage supply conditions. As the supply voltage continues to scale down, traditional cascode topologies are no longer suitable for achieving high dc gains, since they cause a reduction of the voltage swings. To avoid cascoding, dc gains in excess of 100 dB are achieved by cascading three transconductance gain stages. However, this approach causes bandwidth reduction, since each stage inevitably introduces low-frequency poles which require additional compensation capacitors to provide adequate closed-loop stability.

Miller effect to split the low frequency poles and achieve the desired phase margin and transient response.

However, this solution results in bandwidth and slew rate reduction(the gain-bandwidth product is one-quarter as that achievable by a single-stage amplifier)

When the inner OTA stage is the only inverting one, another kind of compensation scheme, termed the reversed NMC (RNMC) is the most suitable option. This technique exploits the same operating principle of the NMC but provides an inherent bandwidth improvement since, as shown in Fig.1,the inner compensation capacitor does not load the output node .

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Indeed, many applications require high-gain OTAs driving loads in the order of hundreds of picofarads in battery-powered equipments, such as high-accuracy ∑△ modulators, flash and pipeline analog-to-digital converters, linear regulators, and active matrix display drivers.

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For both topologies, the design of the compensation network starts from the analysis of the open loop transfer function,which can be obtained by analyzing the equivalent small-signal circuits shown in the same Figs. 2 and 3.

assuming that the dc gain of each stage Av= gm\*ro >>1 and that CL ,Cc1 ,Cc2 >> Coi. Consequently, we will neglect the high-frequency poles due to parasitics.

However, this is not crucial for stability since the zero is still positioned at high frequencies if the coefficient is maintained relatively small. Nevertheless, appropriate biasing schemes can be used to ensure reliable matching.

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The simplified schematic of the mplemented three-stage amplifier compensated using the RNMCFNR technique is shown in Fig. 4. The first stage is made up of a pMOS differential pair (M1–M2) with a current mirror load (M3–M4). The second inverting stage is realized by common source M6–M5, while the last noninverting stage is made up by M7–M10. The feedforward stage is generated exploiting the activeload transistor M10 of the last stage, whose gate is connected to the output of the first stage.

Moreover,with this connection M9–M10 act as a pseudoclass AB output stage able to drive the load capacitor, , with a current much higher than the output branch quiescent current. Asaresult,slew rate is in principle ultimately determined bythe maximum available current from the first stage charging Cc1 and Cc2